Low Power Compressor Based MAC Architecture for DSP Applications

***Abstract*—** This paper presents the low power compressor based Multiply-Accumulate (MAC) architecture for DSP applications. In VLSI, highly computed arithmetic cells
including adders and multipliers are the most copiously used components. Efficient implementation of arithmetic logic units, floating point units and other dedicated functional components are utilized in most of the microprocessors and
digital signal processors (DSPs). Thus in this brief, compressor circuit has been illustrated for the low power applications and also the impact of datapath circuits has
been demonstrated. The proposed low power compressor architecture was applied to MAC unit and compared against the conventional compressor based MAC units and observed
that the proposed architecture has reduced significant amount of leakage power.

**LANGUAGE USED:**

**TOOLS REQUIRED:**

* MODELSIM – Simulation
* XILINX-ISE – Synthesis